PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference P/63610/GPTU18	**FOR FURTHER ACTION**	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/GB 03/01028	International filing date *(day/month/year)* 11.03.2003	Priority date *(day/month/year)* 14.03.2002
International Patent Classification (IPC) or both national classification and IPC H04B10/06		
Applicant MARCONI UK INTELLECTUAL PROPERTY LTD et al		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 5 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 4 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the opinion
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
10.10.2003	10.03.2004
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized Officer De Vries, J Telephone No. +49 89 2399-8949

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/GB 03/01028

I. Basis of the report

1. With regard to the **elements** of the international application *(Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17))*:

Description, Pages

1-12	as originally filed

Claims, Numbers

1-17	received on 12.02.2004 with letter of 09.02.2004

Drawings, Sheets

1/3, 3/3	as originally filed
2/3	received on 12.02.2004 with letter of 09.02.2004

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

   These elements were available or furnished to this Authority in the following language: , which is:

   ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).

   ☐ the language of publication of the international application (under Rule 48.3(b)).

   ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

   ☐ contained in the international application in written form.

   ☐ filed together with the international application in computer readable form.

   ☐ furnished subsequently to this Authority in written form.

   ☐ furnished subsequently to this Authority in computer readable form.

   ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

   ☐ the description, pages:

   ☐ the claims, Nos.:

   ☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)).

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1 - 17
	No:	Claims	
Inventive step (IS)	Yes:	Claims	1 - 17
	No:	Claims	
Industrial applicability (IA)	Yes:	Claims	1 - 17
	No:	Claims	

2. Citations and explanations

   see separate sheet

Re Item V

Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1). Citations : D1 : US-A-6 222 660
D2 : US-A-5 953 690
D3 : US-A-6 157 022

2). The present invention relates to control of bias voltage of avalanche photodiodes.

3a). Attention is directed to D1 which shows a method and apparatus for controlling the bias voltage of an avalanche photodiode (col. 1 lines 5 to 9) by determining various constant power level curves over which the bit error rate is zero but does not discuss the timing of these measurements.
Furthermore, after the optical signal is converted to an electrical signal the error rate of this signal is measured and the bias voltage is adjusted in order to minimise the error rate (col. 3 lines 17 to 21) .

b). Similarly to D1 , in D2 characteristic data curves are stored in a memory containing information of control functions over a range of operating conditions such as varying temperature and power supply voltage levels. This also involves providing a variable avalanche diode bias voltage to achieve the lowest error rate (col. 19 lines 25 to 37 and col 21 lines 12 to 50).The time interval at which the error rate is measured is set according to efficiency but no indication is given as to determining the tendance of the error rate to be increasing or decreasing and to adjust the time period accordingly.

c). In D3 a method and apparatus is shown for controlling the bias voltage of an avalanche photodiode which compensates for temperature variation (see figures 2 and 3).

d). Therefore in the prior art from the Search Report there does not appear to be a disclosure of or hint towards determining the increasing or decreasing tendance of the error rate in order to adjust the sample time period accordingly.

4a). Therefore independent claims 1 (method) and 8 (apparatus) appear to meet the requirements of Articles 33(2) and (3) PCT .

b). The dependent claims 2 to 8 and 9 to 17 also meet the requirements of Articles 33(2) and (3) being respectively dependent upon claims 1 and 8.

5). Concerning the application the description was not amended to conform with the amended claims (see especially statement of invention on page 5 and Rule 5.1(iii)PCT).

CLAIMS

1. A method of controlling the bias voltage of an avalanche photodiode in an optical communications system including forward error correction, the method comprising measuring the error rate in an electrical signal converted from an optical signal by the avalanche photodiode, and adjusting the bias voltage applied to the avalanche photodiode to minimise the error rate in the electrical signal, wherein the error rate is measured over a plurality of sample periods and a determination is made of whether or not the error rate is increasing or decreasing with time.

2. A method according to claim 1, wherein the bias voltage is determined by the value of a counter which is incremented or decremented every sample period, comprising changing the count direction of the counter if the error rate is increasing with time.

3. A method according to claim 2,comprising inhibiting movement of the clock if the error rate is zero.

4. A method according to claim 2 or claim 3, wherein the sample period is determined by a clock tick.

5. A method according to claim 4, wherein the interval between clock ticks is variable.

6. A method according to claim 5, wherein the interval between clock ticks varies in dependence on the measured error rate.

7. A method according to claim 5 or claim 6, comprising a plurality of possible interval lengths, wherein the interval selected is increased if the error rate is below a first level and decreased if the error rate is above a second level.

8. Apparatus for controlling the bias voltage of an avalanche photodiode (APD) in an optical communications system including forward error correction (FEC), comprising an error rate measurer for measuring the error rate in an electrical signal converted from an optical signal by the APD, and an adjustment circuit for adjusting the bias voltage applied to the APD to minimise the measured error rate, wherein the adjustment circuit comprises decision logic for determining whether the error rate is increasing or decreasing with time.

9. Apparatus according to claim 8, wherein the adjustment circuit comprises a counter, the value of which determines the level of the bias voltage, and means for changing the count direction if the decision logic determines that the error rate is increasing.

10. Apparatus according to claim 9, wherein the means for changing the count direction is a toggle.

11. Apparatus according to claim 10, comprising a digital to analog converter for converting the counter value to an analog APD bias voltage.

12. Apparatus according to any of claims 8 to 11, wherein the adjustment circuit comprises an error pulse counter for counting error pulses over a predetermined interval, and a store for holding error counts for a plurality of earlier intervals.

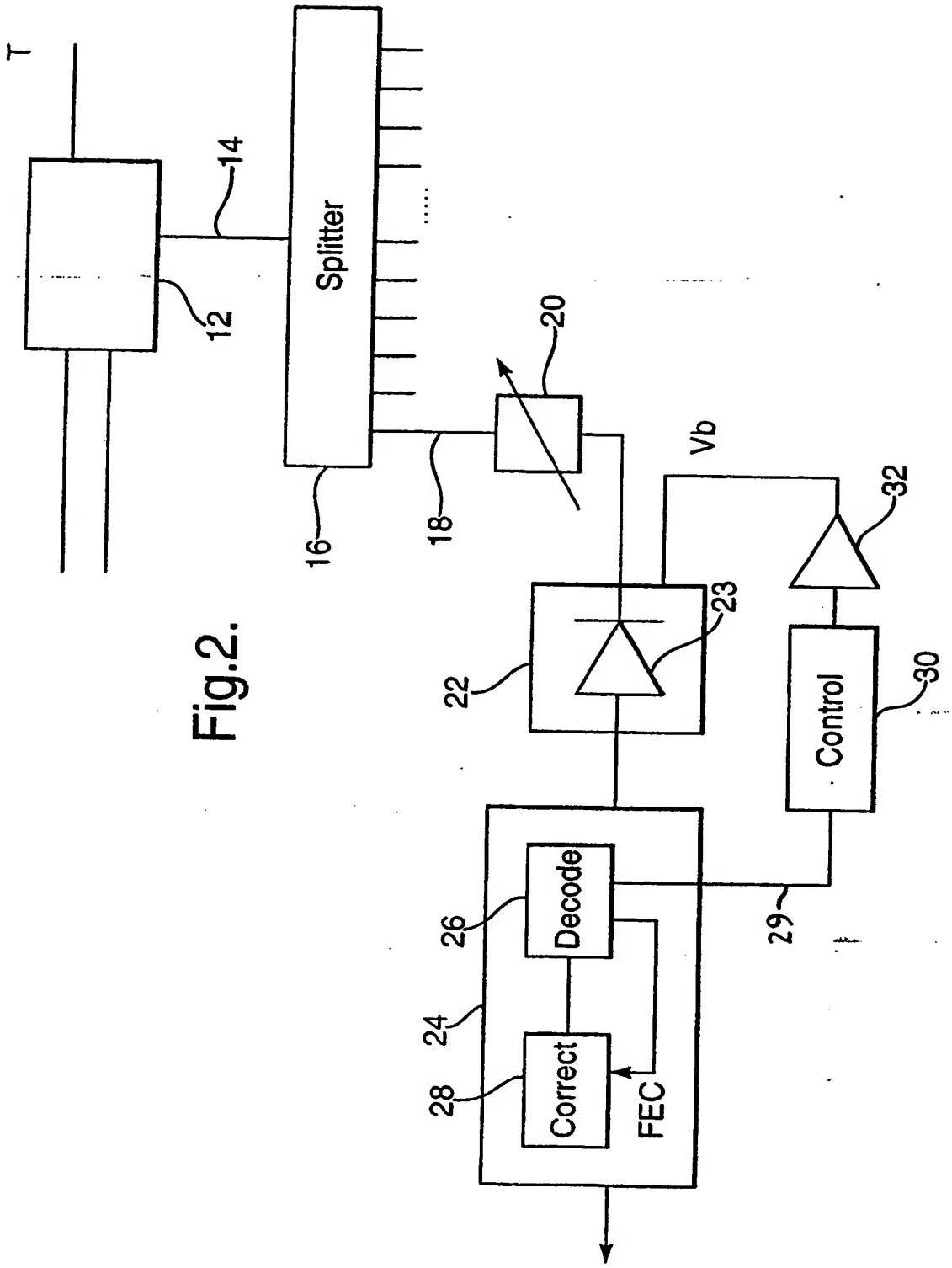
13. Apparatus according to claim 12, wherein the decision logic operates on the error counts held in the store.

14. Apparatus according to claim 12 or 13, comprising means for varying the interval over which error pulses are measured.

15. Apparatus according to claim 14, wherein the interval changing means varies the interval in dependence on the error rate.

16. Apparatus according to claim 14 or 15, wherein the interval varying means varies the interval between one of a plurality of different interval lengths.

17. Apparatus according to any of claims 9 to ~~11~~, comprising an inhibitor for inhibiting movement of the counter if the measured error rate is zero.


T
14
12
Splitter
16
18
20
Vb
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23
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Control
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Decode
26
29
24
Correct
28
FEC

Fig.2.